## REMARKS

The present amendment is submitted in response to the Final Office Action mailed April 19, 2007. Claims 1- 10 are currently pending in the application. In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested.

### 35 U.S.C. §102(b)

Claims 1 – 4 and 6 - 10 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,258,968 – Matsuda et al – hereinafter Matsuda.

Applicants respectfully traverse the rejection of claims 1 – 4 and 6 – 10 under 35 U.S.C. §102(b), however, Claim 1 has been amended.

Applicant appreciates the courtesy granted to Applicant's attorney, Michael A. Scaturro (Reg. No. 51,356), during a telephonic interview conducted on Tuesday, May 29, 2007. During the telephonic interview, Applicant's attorney proposed an amendment to Claim 1 that Applicant's Attorney believes will make it allowable over the cited reference, Matsuda.

Upon reviewing the proposed amendment, the Examiner concluded that the proposed amendment makes Claim 1 distinguishable over at least the cited reference, Matsuda.

Claim 1, as presented to the Examiner recites:

1. An Optical disk system comprising at least one photo detector for detecting at least a part of said optical disk and in response generating detection signals and comprising at least one amplifier for amplifying detection signals and comprising at least one slicer for slicing amplified detection signals and comprising at least one delay-difference detector for detecting delay differences in sliced amplified detection signals, characterized in that said delay-difference detector is delaylineless and comprises combinatorial-logic circuits and sequential-logic circuits, said combinatorial-logic circuits for receiving output signals from said several sub-detectors and for generating signal pairs to be supplied to one of a first pair or a second pair of sequential logic circuits, said sequential logic circuits generating sequential logic circuit output signal pairs to be supplied directly to at least one analog adder/subtractor for adding/subtracting said sequential logic circuit output signal pairs.

As shown above, Claim 1 as amended recites that the sequential logic circuits generate sequential logic circuit outputs signal pairs that are supplied directly to at least one analog adder/subtractor for adding/subtracting the sequential logic circuit output signal pairs. As pointed out by the Examiner, the reference, Matsuda, illustrates in FIG. 9 that the delay difference detector 110 is comprised of combinational logic circuits 115, 116 whose output is supplied to sequential logic circuits 111, 112, 113, 114, whose output is supplied to still further sequential logic circuits 117, 118. As such, Matsuda does no teach sequential logic circuit outputs signal pairs that are supplied directly to at least one analog adder/subtractor for adding/subtracting the sequential logic circuit output signal pairs.

Accordingly, it is believed that Applicant's Claim 1 recites patentable subject matter, and therefore, withdrawal of the rejections with respect to Claim 1 and allowance thereof is respectfully requested.

Claims 2 – 4 depend from Claim 1, and therefore include the limitations of Claim 1. Hence, for the same reasons given above for Claim 1, Claims 2 – 4 are believed to contain patentable subject matter. Accordingly, withdrawal of the rejection with respect to Claims 2 – 4 and allowance thereof are respectfully requested.

Independent Claims 6 and 9 as amended, recite similar subject matter as Claim 1 and therefore contain the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claims 6 and 9 are believed to contain patentable subject matter.

Accordingly, withdrawal of the rejections with respect to Claims 6 and 9 and allowance thereof are respectfully requested.

Claims 7 – 8 depend from Claim 6, and therefore include the limitations of Claim 6. Hence, for the same reasons given above for Claim 6, Claims 7 – 8 are believed to contain patentable subject matter. Accordingly, withdrawal of the rejection with respect to Claims 7 – 8 and allowance thereof are respectfully requested.

Claim 10 depends from Claim 9, and therefore include the limitations of Claim 9. Hence, for the same reasons given above for Claim 9, Claim 10 is believed to contain patentable subject matter. Accordingly, withdrawal of the rejection with respect to Claim 10 and allowance thereof are respectfully requested.

### *35 U.S.C. §103(a)*

In the Office Action, Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Matsuda, in view of U.S. Patent No. 6,940,799 to Ma et al.

Claim 5 depends from Claim 1 and therefore contain the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claim 5 is believed to be allowable over Matsuda in view of Mai.

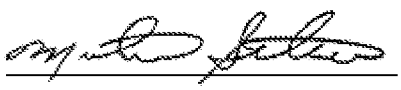
Accordingly, applicant respectfully request withdrawal of the rejection under 35 U.S.C. §103(a) with respect to Claim 5 and allowance thereof is respectfully requested.

## Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1 - 10 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Michael Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-333-9643.

Respectfully submitted,



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